CLAIMS

1. A semiconductor structure comprising:

a monocrystalline silicon substrate;

an amorphous oxide material overlying the monocrystalline silicon substrate;

a monocrystalline perovskite oxide material overlying the amorphous oxide material;

a monocrystalline compound semiconductor material overlying the monocrystalline perovskite oxide material; and

a composite transistor comprising

a first transistor having first active regions formed at least in part in a silicon portion of the semiconductor structure,

a second transistor having second active regions formed at least in part in a monocrystalline compound semiconductor portion of the semiconductor structure, and

a mode control terminal for controlling the first transistor and the second transistor.

2. The semiconductor structure of claim 1 wherein the first transistor comprises a first field effect transistor having a monocrystalline silicon source region and a monocrystalline silicon drain region formed in the monocrystalline silicon substrate and the second transistor comprises a second field effect transistor having a monocrystalline compound semiconductor source region and a monocrystalline compound semiconductor drain region formed in the monocrystalline compound semiconductor material.

3. The semiconductor structure of claim 2 wherein the first transistor comprises a first gate associated with the monocrystalline silicon drain region and the monocrystalline silicon source region and coupled with the mode control terminal and the second transistor comprises a second gate associated with the monocrystalline compound semiconductor source region and the monocrystalline compound semiconductor drain region and coupled with the mode control terminal.

4. The semiconductor structure of claim 3 wherein the mode control terminal is configured to receive a signal to select one of a cut-off mode and a saturated mode for the first transistor and the second transistor.

5. The semiconductor structure of claim 2 further comprising:

a first multi-fingered gate separating the monocrystalline silicon source region and the monocrystalline silicon drain region; and

one or more switches for selectively actuating fingers of the first multi-fingered gate.

6. The semiconductor structure of claim 5 further comprising:

a second multi-fingered gate separating the monocrystalline compound semiconductor source region and the monocrystalline compound semiconductor drain region; and

one or more switches for selectively actuating fingers of the second multi-fingered gate.

7. The semiconductor structure of claim 6 further comprising:

a processor formed in the monocrystalline silicon substrate and coupled with the first multi-fingered gate and second multi-fingered gate to provide control signals to control selective actuation of the fingers of the first multi-fingered gate and second multi-fingered gate.

8. The semiconductor structure of claim 1 further comprising:

a signal input electrically coupled with a first active region of the first transistor and a first active region of the second transistor; and

a signal output electrically coupled with a second active region of the first transistor and a second active region of the second region.

9. The semiconductor structure of claim 1 further comprising

a silicon bipolar junction transistor formed at least in part in the monocrystalline silicon substrate; and

a heterojunction bipolar transistor formed at least in part in the monocrystalline compound semiconductor material.

10. The semiconductor structure of claim 9 wherein the silicon bipolar junction transistor and the heterojunction bipolar transistor each comprise a base contact electrically coupled with the mode control terminal.

11. A semiconductor structure comprising:

a monocrystalline silicon substrate;

an amorphous oxide material overlying the monocrystalline silicon substrate;

a monocrystalline perovskite oxide material overlying the amorphous oxide material;

a monocrystalline compound semiconductor material overlying the monocrystalline perovskite oxide material;

a silicon transistor formed at least in part in the monocrystalline silicon substrate;

a compound transistor formed at least in part in the monocrystalline compound semiconductor material;

a switch to selectively couple the silicon transistor and the compound transistor in response to a control signal; and

a control circuit configured to provide the control signal.

12. The semiconductor structure of claim 11 wherein the control circuit is formed at least in part of a silicon portion of the semiconductor structure.

13. The semiconductor structure of claim 11 further comprising:

a first input associated with a gate of the silicon transistor and configured to receive a first input signal;

a second input associated with a gate of the compound transistor and configured to receive a second input signal;

an output configured to provide a mixed signal when the switch receives a control signal associated with a mixer configuration; and

a matching network between source/drains of the silicon transistor and the compound transistor and the output.

14. The semiconductor structure of claim 11 further comprising:

a bias network to selectively bias the silicon transistor and the compound transistor as an amplifier when the switch receives a control signal associated with an amplifier configuration.

15. The semiconductor structure of claim 11 wherein the silicon transistor comprises a gate, a first source/drain connection and a second source/drain connection coupled with the switch and the compound transistor comprises a gate, a first source/drain connection coupled with the switch and a second source/drain connection.

16. The semiconductor structure of claim 15 wherein the switch is responsive to a first control signal value for coupling the second source/drain connection of the silicon transistor and the first source drain/ connection of the compound transistor.

17. The semiconductor structure of claim 16 wherein the switch is responsive to a second control signal value for coupling the second source/drain connection of the silicon transistor to a ground potential and for coupling the first source/drain connection of the compound transistor to an output network.

18. The semiconductor structure of claim 17 further comprising:

a matching network configured to combine an output signal from the first source/drain connection of the silicon transistor and another output signal from the first source/drain of the compound transistor at an output.

19. The semiconductor structure of claim 18 further comprising bias circuits for selectively biasing gates of the silicon transistor and the compound transistor.

20. The semiconductor structure of claim 11 wherein the switch comprises a micro-electro-mechanical system (MEMS) switch.

21. The semiconductor structure of claim 11 wherein the control circuit comprises a digital logic circuit formed at least in part in the monocrystalline silicon substrate.

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22. A semiconductor structure comprising:

a monocrystalline silicon substrate;

an amorphous oxide material overlying the monocrystalline silicon substrate;

a monocrystalline perovskite oxide material overlying the amorphous oxide material;

a monocrystalline compound semiconductor material overlying the monocrystalline perovskite oxide material;

one or more silicon transistors formed at least in part in the monocrystalline silicon substrate;

one or more compound transistors formed at least in part in the monocrystalline compound semiconductor material; and

switches associated with respective transistors of the one or more silicon transistors and the one or more compound transistors, the switches receiving control signals for selectively coupling the respective transistors to one of the signal input circuit and the signal output circuit.

23. The semiconductor structure of claim 22 further comprising:

a control circuit coupled with the switches to provide the control signals.

24. The semiconductor structure of claim 23 wherein the control circuit is formed at least in part in the monocrystalline silicon substrate.

25. The semiconductor structure of claim 22 further comprising a matching network configured to combine signals from two or more transistors.

26. A configurable transistor device comprising:

one or more silicon transistors;

one or more compound semiconductor transistors formed in a monolithic semiconductor device with the one or more silicon transistors; and

switching means for selectively combining the one or more silicon transistors and the one or more compound transistors to tailor electrical parameters of the configurable transistor device.

27. The configurable transistor device of claim 26 wherein the switching means comprises:

semiconductor switch means for coupling two or more devices in response to a control signal.

28. The configurable transistor device of claim 26 further comprising:

control means for controlling the switching means.

29. The configurable transistor device of claim 26 further comprising:

processor means responsive to data and instructions for controlling the switching means.

30. A composite transistor comprising:

a silicon transistor formed at least in part in a silicon portion of an integrated circuit; and

a compound semiconductor transistor formed at least in part in a compound semiconductor portion of the integrated circuit, the compound semiconductor transistor and the silicon transistor having at least one electrically common terminal.

31. The composite transistor of claim 30 wherein the compound semiconductor transistor has a gate and the silicon transistor has a gate electrically coupled to the gate of the compound semiconductor transistor.

32. The composite transistor of claim 30 wherein the compound semiconductor transistor has one or more source/drain region and the silicon transistor has at least one source/drain region electrically coupled to a source/drain region of the compound semiconductor transistor.

33. The composite transistor of claim 30 further comprising:

additional silicon transistors and additional compound semiconductor transistors which may be configured with the silicon transistor and the compound semiconductor transistor to optimize one or more electrical parameters of the composite transistor.

34. The composite transistor of claim 33 further comprising:

one or more switch devices to selectively configure the additional silicon transistors and the additional compound semiconductor transistors with the silicon transistor and the compound semiconductor transistor.

35. A configurable mixer and amplifier comprising:

a silicon transistor;

a compound semiconductor transistor formed in a common semiconductor structure with the silicon transistor; and

a switching device including

a switch which selectively couples a source/drain region of the silicon transistor and one of a source/drain region of the compound semiconductor transistor in an amplifier mode and ground potential in a mixer mode, and

a switch which selectively couples the source/drain region of the compound semiconductor transistor and an output in the mixer mode.

37. A semiconductor structure comprising:

a monocrystalline silicon substrate;

an amorphous oxide material overlying the monocrystalline silicon substrate;

a monocrystalline perovskite oxide material overlying the amorphous oxide material; and

a monocrystalline compound semiconductor material overlying the monocrystalline perovskite oxide material;

at least one configurable transistor formed at least in part in the monocrystalline compound semiconductor material; and

a control circuit electrically coupled with the transistor and formed at least in part in a silicon portion of the semiconductor structure.

38. The semiconductor structure of claim 37 further comprising:

at least one silicon transistor electrically coupled with the control circuit and formed at least in part in the silicon portion of the semiconductor structure.

39. The semiconductor structure of claim 37 wherein the at least one configurable transistor is configurable in response to a signal received from the control circuit.

40. A process for fabricating a semiconductor structure comprising:

providing a monocrystalline silicon substrate;

depositing a monocrystalline perovskite oxide film overlying the monocrystalline silicon substrate, the film having a thickness less than a thickness of the material that would result in strain-induced defects;

forming an amorphous oxide interface layer containing at least silicon and oxygen at an interface between the monocrystalline perovskite oxide film and the monocrystalline silicon substrate;

epitaxially forming a monocrystalline compound semiconductor layer overlying the monocrystalline perovskite oxide film;

forming a configurable transistor at least in part in the monocrystalline compound semiconductor material.

41. The process of claim 40 wherein forming the configurable transistor comprises:

forming one or more monocrystalline compound semiconductor transistors at least in part in the monocrystalline semiconductor material; and

forming one or more silicon transistors at least in part in a silicon portion of the semiconductor structure.

42. The process of claim 41 wherein forming the configurable transistor comprises:

electrically coupling the one or more monocrystalline compound semiconductor transistors and the one or more silicon transistors.

43. The process of claim 41 wherein forming the configurable transistor comprises:

forming the one or more silicon transistors in the monocrystalline silicon substrate.

44. The process of claim 41 wherein forming the configurable transistor comprises:

forming the one or more silicon transistors in an epitaxial silicon layer overlying at least a portion of the monocrystalline silicon substrate.

45. The process of claim 41 further comprising:

forming a control circuit in at least a portion of the monocrystalline silicon substrate of the semiconductor structure.

46. The process of claim 41 further comprising:

forming a control circuit in at least a portion of the monocrystalline compound semiconductor layer of the semiconductor structure.

47. The process of claim 41 wherein forming the configurable transistor comprises:

forming at least one transistor having a multi-fingered gate separating monocrystalline semiconductor source/drain regions.

48. The process of claim 41 further comprising:

forming one or more switch devices electrically coupled with the multi-fingered gate; and

forming a control circuit electrically coupled with the one or more switch devices.